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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/875,255	06/07/2001	Yoshikazu Fukuhara	43890-521	4611

7590 11/02/2004

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EXAMINER	
BURD, KEVIN MICHAEL	

ART UNIT	PAPER NUMBER
2631	

DATE MAILED: 11/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/875,255	FUKUHARA, YOSHIKAZU	
	Examiner	Art Unit	
	Kevin M. Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4 and 7* is/are rejected.

7)☒ Claim(s) *3,5 and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 October 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/7/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on 6/7/2001 is being considered by the examiner.

Drawings

2. Figure 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(e) as being anticipated by Matsuda et al (US 5,883,533).

Regarding claim 1, Matsuda discloses a digital phase lock loop (PLL) shown in figure 1. A selector 50 selects a first timing signal or a second timing signal (column 2, lines 11-15). A comparator 61 detects the phase difference between the selected timing signal and an internal timing signal that is output from the frequency divider 60. The phase difference is output (column 2, lines 21-25). The phase difference is received in the holdover circuit 63. The hold over circuit acts as a selector for outputting the phase corrected data (column 2, lines 26-30) or outputs a hold over signal when a hold over mode is set (column 2, lines 38-47). A VCO 64 creates a clock signal in response to the output from holdover circuit 63. The VCO outputs an internal timing signal that will be fed to the comparator 61.

Regarding claim 2, a controller controls the holdover circuit while a change between timing signals is occurring (column 2, lines 38-59).

Regarding claim 4, the phase of the timing signals will be phase adjusted according to the output of the phase comparator.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsuda et al (US 5,883,533) in view of the instant application's disclosed prior art.

Regarding claim 7, Matsuda discloses a digital phase lock loop (PLL) shown in figure 1. A selector 50 selects a first timing signal or a second timing signal (column 2, lines 11-15). A comparator 61 detects the phase difference between the selected timing signal and an internal timing signal that is output from the frequency divider 60. The phase difference is output (column 2, lines 21-25). The phase difference is received in the holdover circuit 63. The hold over circuit acts as a selector for outputting the phase corrected data (column 2, lines 26-30) or outputs a hold over signal when a hold over mode is set (column 2, lines 38-47). A VCO 64 creates a clock signal in response to the output from holdover circuit 63. The VCO outputs an internal timing signal that will be fed to the comparator 61. Matsuda does not disclose using the PLL in a digital PBX. However, the instant application's disclosed prior art discloses a digital PBX uses the conventional PLL as shown in figure 10. It would have been obvious for one of ordinary skill in the art at the time of the invention to use the PLL of Matsuda in the convention PBX shown in figure 10 and described in pages 1 and 2 of the instant. The PBX is the one of the most modern and fully digitized phone systems and requires accurate error-free timing signals.

Allowable Subject Matter

5. Claims 3, 5 and 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Alder et al (US 5,572,167) discloses a phase lock loop circuit that selects a first or second timing signal to be input to the PLL. This circuit includes a holdover mode (abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Thursday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Burd
10/29/2004

KEVIN BURD
PATENT EXAMINER